WHAT IS CLAIMED IS:

1. A memory system, comprising:

a control circuit having a data register for storing write data, said control circuit controlling write operation of the memory system; and

memory means having a plurality of memory cells, for latching a data group composed of data of predetermined bits transferred from the data register, for writing the latched data group in the memory cells, and for outputting a collective verify signal when all the data of the data group have been written;

wherein whenever the collective verify signal is outputted by said memory means, said control circuit transfers a new data group to said memory means to allow said memory means to latch and write the transferred new data group therein and transfers the collective verify signal to said control circuit whenever the new latched data group has been written, the write operation being repeated in sequence.

2. The memory system of claim 1, wherein the memory cells are divided into a plurality of erase blocks each composed of a plurality of memory cells, data stored in each of said erase blocks are erased simultaneously, and a plurality of data groups are written in each of said erase blocks.

3. The memory system of claim 2, wherein said memory means is of NAND type EEPROM, each of said erase blocks is divided into a plurality of pages, and data are written in each of the erase blocks by sequentially writing data for one page transferred from said control circuit plural times in sequence.

4. The memory system of claim 2, wherein said memory means is of NOR type EEPROM, each of said erase blocks is divided into a plurality of pages, and data are written in the collective erase block by sequentially writing data

for one page transferred from said control circuit plural times in sequence.

5. A memory system, comprising:

a control circuit having a data register for storing write data, said control circuit controlling operation of the memory system; and

a plurality of memory means each having a plurality of memory cells, each for executing data write operation for latching a data group composed of data of predetermined bits transferred from the data register and for writing the latched data group in the memory cells, and executing write verify operation for checking whether all the data of the data group have been written correctly and for outputting a collective verify signal when all the data of the data group have been written completely;

wherein whenever said control circuit receives the collective verify signal outputted from one of said memory means, said control circuit executes a data transfer operation for transferring a new data group to one of said memory means and for allowing one of said memory means to latch the new data group, and said one of said memory means writes the latched new data group therein, whenever said one of said memory means executes the write operation for allowing one of said memory means to write new latched data group therein completely, said one of memory means transferring the collective verify signal to said control circuit, said control circuit executing another data transfer operation for transferring another new data group to another of said memory means during the one of memory means executes the write and verify operation, the data write operation to one of said memory means and the data transfer operation to another of said memory means being executed simultaneously in parallel to each other and repeatedly.

6. The memory system of claim 5, wherein the number of said memory means is two, and when the data transfer operation is being executed to one of said memory means,

the write and verify operation is executed to the other of said memory means in parallel to the data transfer operation of said one of said memory means, and when the write and verify operation is being executed to one of said memory means, the data transfer operation is executed to the other of said memory means in parallel to the write verify operation of said one of said memory means, the operation as above being repeated in sequence.

7. The memory system of claim 5, wherein the memory cells are divided into a plurality of erase blocks each composed of a plurality of memory cells, data stored in each of said erase blocks are erased simultaneously, and a plurality of data group are written in each erase block.

8. The memory system of claim 6, wherein the memory cells are divided into a plurality of erase blocks each composed of a plurality of memory cells, data stored in each of said erase blocks are erased simultaneously, and a plurality of data group are written in each erase block.

9. The memory system of claim 7, wherein each of said memory means is of NAND type EEPROM, said erase block is divided into a plurality of pages, and data are written in the erase block by sequentially writing data for one page transferred from said control circuit plural times in sequence.

10. The memory system of claim 8, wherein each of said memory means is of NAND type EEPROM, said erase block is divided into a plurality of pages, and data are written in the erase block by sequentially writing data for one page transferred from said control circuit plural times in sequence.

11. The memory system of claim 7, wherein each of said memory means is of NOR type EEPROM, said erase block is divided into a plurality of pages, and data are written in the erase block by sequentially writing data for one

page transferred from said control circuit plural times in sequence.

12. The memory system of claim 8, wherein each of said memory means is of NOR type EEPROM, said erase block is divided into a plurality of pages, and data are written in the erase block by sequentially writing data for one page transferred from said control circuit plural times in sequence.

13. A cache memory system, comprising:

a main memory, a cache memory, and a control circuit for controlling data transfer operation between said main memory and said cache memory, and

wherein said main memory is comprised of a plurality of erase blocks each having memory cells of predetermined bits, and outputs an erase verify signal whenever all bits of one of the erase blocks have been erased; and

wherein when accessed data are not present in said cache memory at cache mishit, said control circuit erases data of one of said erase blocks; and after the data have been erased completely and thereby the erase verify signal has been outputted, said control circuit executes data rewrite operation for rewriting data in said cache memory into the erased erase block.

14. The cache memory system of claim 13, wherein after the data rewrite operation, said control circuit executes copy operation for copying object data in said main memory into a vacant space in said cache memory obtained by the rewrite operation.

15. The cache memory system of claim 14, wherein after the copy operation, said control circuit executes rewrite operation for rewriting the copied data in said main memory to external write data.

16. The cache memory system of claim 13, wherein in the rewrite operation, said control circuit controls the data transfer operation from said cache memory to one of said erase blocks in such a way that data are divided into a plurality of divided block data of predetermined bits and the divided block data are transferred plural times.

17. The cache memory system of claim 14, wherein in the rewrite operation, said control circuit controls the data transfer operation from said cache memory to one of said erase blocks in such a way that data are divided into a plurality of divided block data of predetermined bits and the divided block data are transferred plural times.

18. The cache memory system of claim 15, wherein in the rewrite operation, said control circuit controls the data transfer operation from said cache memory to one of said erase blocks in such a way that data are divided into a plurality of divided block data of predetermined bits and the divided block data are transferred plural times.

19. The cache memory system of claim 16, wherein said main memory executes write operation whenever the divided block data are transferred, and outputs a write verify signal whenever all the divided block data have been written completely; and said control circuit transfers the succeeding divided block data from said cache memory to said main memory whenever all the divided block data have been written completely and thereby the write verify signal has been outputted.

20. The cache memory system of claim 17, wherein said main memory executes write operation whenever the divided block data are transferred, and outputs a write verify signal whenever all the divided block data have been written completely; and said control circuit transfers the succeeding divided block data from said cache memory to said main memory whenever all the divided block data have

been written completely and thereby the write verify signal has been outputted.

21. The cache memory system of claim 18, wherein said main memory executes write operation whenever the divided block data are transferred, and outputs a write verify signal whenever all the divided block data have been written completely; and said control circuit transfers the succeeding divided block data from said cache memory to said main memory whenever all the divided block data have been written completely and thereby the write verify signal has been outputted.

22. The cache memory system of claim 19, wherein said main memory is of NAND type EEPROM, said erase block is divided into a plurality of pages, and data are written in the erase block by sequentially writing data for one page plural times in sequence.

23. The cache memory system of claim 20, wherein said main memory is of NAND type EEPROM, said erase block is divided into a plurality of pages, and data are written in the erase block by sequentially writing data for one page plural times in sequence.

24. The cache memory system of claim 22, wherein said main memory is of NAND type EEPROM, said erase block is divided into a plurality of pages, and data are written in the erase block by sequentially writing data for one page plural times in sequence.

25. The cache memory system of claim 19, wherein said main memory is of NOR type EEPROM, said erase block is divided into a plurality of pages, and data are written in the erase block by sequentially writing data for one page plural times in sequence.

26. The cache memory system of claim 20, wherein said main memory is of NOR type EEPROM, said erase block is

divided into a plurality of pages, and data are written in the erase block by sequentially writing data for one page plural times in sequence.

27. The cache memory system of claim 22, wherein said main memory is of NOR type EEPROM, said erase block is divided into a plurality of pages, and data are written in the erase block by sequentially writing data for one page plural times in sequence.